forming a source/drain diffused layer in a substrate for a transistor;

forming a dummy diffused layer in the substrate;

covering at least a portion of the dummy diffused layer with an anti-silicidation film; and

forming a silicide layer on the surface of the source/drain diffused layer.

19. (New) A method of making a semiconductor device comprising:

forming a source/drain diffused layer in a substrate for a transistor;

forming a dummy diffused layer in the substrate;

covering at least a portion of the dummy diffused layer with a dummy gate electrode; and

forming a silicide layer on the surface of the source and drain diffused layers.

REMARKS

Applicants thank Examiners Owens and Loke for their courtesy extended to Applicants and Applicants' representative during an interview on October 2, 2002. During the interview, the Examiner indicated that the rejection under Hyneck (U.S. Pat. 5,464,996) and the rejection under Oh et al. (U.S. Pat. 5,867,434) would not be maintained. As the Examiner indicated that it is not necessary for the Applicant to provide a separate record of the substance of the interview, in the interest of expediency, no further discussion of the interview is provided.

I. Introduction

Claims 1-19 are pending in the above application.

Claims 1-4, 7 and 8 stand rejected under 35 U.S.C. §103.

Claims 12 and 13 stand allowed.

Claims 5, 6, 9, 10 and 11 stand objected to for containing allowable subject matter but being dependent upon a rejected claim.

Claims 14-19 are newly added.

Claims 1, 4, 8, 12, 18 and 19 are the independent claims.

II. Amendment

The drawings have been amended to add label "Prior Art" to Figures 15-19 as requested by the Examiner.

The title has been amended as requested by the Examiner.

Claim 4 has been amended to remove unnecessary language.

Claims 14-19 have been added.

No new matter has been added.

III. Prior Art Rejections

Claims 1-3 stand rejected under 35 U.S.C. §103 as being unpatentable over Hyneck (U.S. Pat. 5,464,996) as set forth on pages 2-3 of the Office Action.

Claims 4, 7 and 8 stand rejected under 35 U.S.C. §103 as being unpatentable over Oh et al. (U.S. Pat. 5,867,434) (hereafter "Oh") as set forth on pages 3-4 of the Office Action.

As it is Applicants understanding, based on the interview, that neither the rejection under Hyneck nor the rejection under Oh will be maintained, no further response is believed to be necessary.

IV. New Claims

New claims 14-15 depend on claim 1 and thus are patentable at least for the same reasons as claim 1. Likewise, claims 16-17 depend on claim 4 and thus are patentable at least for the same reasons as claim 4.

New claims 18-19 are method claims which address a method of making a semiconductor device. As the prior art of record is not believed to disclose or suggest all of the limitations of method claims 18 and 19, claims 18 and 19 are believed to be patentable.

V. Conclusion

Accordingly, it is urged that the application is in condition for allowance, an indication of which is respectfully solicited.

If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

Respectfully submitted,

McDERMOTT, WILL & EMERY

Date: October 8, 2002

By: _____

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APPENDIX

IN THE DRAWINGS:

Please amend Figs. 15-19 to add the label "Prior Art". The amendments are shown in the attached Letter to the Draftsman.

IN THE TITLE

Please delete the title and insert therein:

--A SEMICONDUCTOR DEVICE HAVING NOISE IMMUNITY--.

IN THE CLAIMS:

Please amend claim 4 and add new claims 14-19 as follows:

4. (Amended) A semiconductor device comprising:

a substrate;

a source/drain diffused layer formed in the substrate for a transistor; and

a dummy diffused layer formed in the substrate;

wherein the source/drain diffused layer has its surface silicided, and

wherein the dummy diffused layer has its surface covered with a dummy gate electrode at least partially[, the dummy gate electrode having the same structure as a gate electrode for the transistor].

14. (New) The device of claim 1, wherein the dummy diffused layer is located between a circuit block and another circuit block.

15. (New) The device of claim 1, wherein the dummy diffused layer is not electrically coupled to another component via an interconnect.

16. (New) The device of claim 4, wherein the dummy diffused layer is located between a circuit block and another circuit block.

17. (New) The device of claim 4, wherein the dummy diffused layer is not electrically coupled to another component via an interconnect.

18. (New) A method of making a semiconductor device comprising:

forming a source/drain diffused layer in a substrate for a transistor;

forming a dummy diffused layer in the substrate;

covering at least a portion of the dummy diffused layer with an anti-silicidation film; and

forming a silicide layer on the surface of the source/drain diffused layer.

19. (New) A method of making a semiconductor device comprising:

forming a source/drain diffused layer in a substrate for a transistor;

forming a dummy diffused layer in the substrate;

covering at least a portion of the dummy diffused layer with a dummy gate electrode; and

forming a silicide layer on the surface of the source and drain diffused layers.